Thermal and Electrical Characterization of Materials for Phase-Change Memory Cells†

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The thermal properties of the phase-change chalcogenide alloy $Ge_2Sb_2Te_5$ in its three phases (amorphous, cubic, and hexagonal) and of Si_3N_4 and SiO_2 have been studied to obtain reliable values for device modeling. Thermal conductivity was determined, along with a quantitative estimation of the thermal resistances of the layers' interfaces, not negligible for highly scaled devices. Electrical resistivity of the chalcogenide material has also been investigated during the phase transition by in situ measurement at constant heating rate.

Introduction

A phase-change memory (PCM) is a nonvolatile memory in which the logic data are stored as a different state of a phase-change material. The memorization process consists of crystallization or amorphization of a small area of the cell by a suitable heating−quenching sequence, provided by passing a programming current through the phase-change material. Read operation is performed by sensing the cell's resistivity that is very high when the active area is in its amorphous state and much lower when it is crystallized. These devices exhibit several advantages over existing "flash" technology nonvolatile memories, namely, a faster write speed, higher cyclability, and better scalability down to and beyond the 45 nm technology node.[1,2] The chalcogenide alloy $Ge_2Sb_2Te_5$ is an ideal candidate for such devices because of its fast (≈100 ns), reversible switching capability and the large difference in resistivity between the amorphous and crystalline phases.

The constant demand for high-speed, high-density nonvolatile data storage devices is urging the investigation of such materials for design, modeling, and prototyping. In this work, materials potentially interesting for memory cells will be investigated, namely, the phase-change chalcogenide $Ge_2Sb_2Te_5$ (GST) in its different phases and insulators, focusing on two physical properties of such materials: the thermal conductivity that affects heat dissipation behavior inside the memory cell and the electrical resistivity that determines the resistance of the active area of the cell. Because the thickness of the chalcogenide layer in actual PCM devices is a few tens of nanometers, experiments have been carried out on *thin* films of thickness below 1 μm.

† Part of the special section "2008 European Conference on Thermophysical Properties".

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Experimental

Two kinds of experiments have been carried out. For each of them, a different preparation will be described.

Thermal Characterization. The technique employed for determining the thermal conductivity is the 3ω method by Cahill.[3] A metal strip is deposited on top of the thin film to be investigated; a current is passed in the strip, causing a known heat power P to be generated; the heat diffuses in the underlying layer and causes a temperature rise ΔT on the metal strip itself. The thermal resistance of the material is determined from the known power P and the measured ΔT by a three-dimensional analytical heat transfer model[4] that takes into account the geometrical configuration as well as the finite thickness of the silicon substrate for low-frequency behavior. Instead of heating by a continuous current, a sinusoidal current at frequency ω is used. Both the power generated and the temperature rise on the strip vary at frequency 2ω. Because the metal strip has a temperature coefficient of resistivity, its resistance varies at frequency 2ω as well. The voltage drop across the heater consists of two components, at frequencies ω and 3ω. The temperature rise is calculated from the measurement of both components (by means of a lock-in amplifier). The excitation current frequency is between some tens of hertz to a few kilohertz. To measure low resistivity samples, to ensure electrical insulation between the metal strip and the sample, a dielectric layer had to be interposed between them. During the measurement the sample is placed in a vacuum chamber so that the only heat transfer mechanism is conduction; radiation is negligible for the measured temperature rises ($\Delta T < 2$ °C). The sample's back is placed in contact with a large copper heat sink by thermal grease to comply with the boundary condition of the heat transfer model $T_{back} = T_{room}$. All measurements were performed at room temperature.

Sample preparation was accomplished by depositing thin films of SiO_2 and Si_3N_4 on a silicon substrate and $Ge_2Sb_2Te_5$ on top of an inert substrate (SiO_2 on bulk Si). The GST samples were additionally capped with evaporated SiO_2 for electrical insulation. A metal strip (Au), of thickness $d = 220$ nm, length $l = 1$ mm, and width $w = 20$ μm, was deposited by evaporation and defined by a photolithographic process, along with four

10.1021/je800770s CCC: $40.75 © 2009 American Chemical Society
Published on Web 04/01/2009

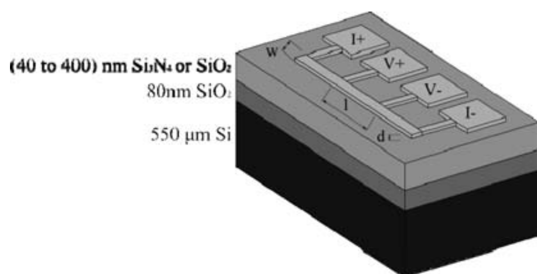

Figure 1. Layout of the SiO_2 and Si_3N_4 samples for 3ω measurement.

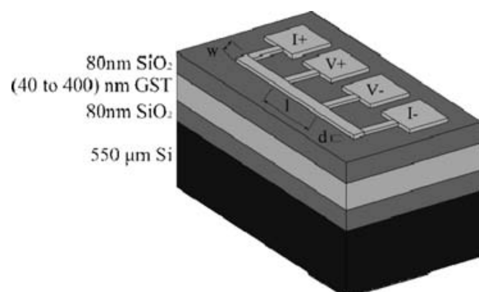

Figure 2. Layout of the GST samples for 3ω measurement.

metal pads to provide connection to the sample holder of the instrument. A sample layout is shown in Figure 1 for the SiO_2 and Si_3N_4 samples and in Figure 2 for $Ge_2Sb_2Te_5$ samples.

It must be pointed out that for these thin films the effect of layer interfaces on the apparent thermal conductivity cannot be neglected. The interface between layers, which acts as a barrier to heat diffusion, affects the measurement in such a way that the measured (apparent) thermal conductivity exhibits a dependence on the layer thickness.[5,6] In the present work, this effect has been taken into account in terms of an additional thermal interfacial resistance R_i. To estimate its value, we measured the thermal resistance R of samples of different thickness t and extrapolated the constant contribution of thermal resistance obtained at $t = 0$. The thermal conductivity of the evaporated silicon dioxide layer has been measured at first because SiO_2 was used as the capping layer to allow the measurement of low resistivity samples. Different SiO_2 layers have been deposited on Si/SiO_2 buffer. In this case, the intrinsic thermal conductivity λ, thickness independent, is derived from formula 1

$$\lambda = \frac{t}{R - R_i - R_{SiO_2}} \qquad (1)$$

where R_{SiO_2} is the thermal resistance of the buffer layer.

Electrical Characterization. The electrical resistivity of the phase change material has been investigated by the four-probe van der Pauw method.[7] For a thin film of thickness t, the resistivity ρ is given by (2)

$$\rho = \frac{\pi}{\ln 2} t \frac{\sum_{i=1}^{8} V_i}{I} \qquad (2)$$

where I is the current supplied by the first pair of probes, and V_i are the voltages measured across the other two probes in eight measurements performed through all possible combinations of probe positions. In comparison with other resistivity measurement techniques, the measurement by the van der Pauw method lessens the effect of nonidealities as nonhomogeneities of the film and geometrical effects of the sample shape and probe positioning, as long as the probes are placed close to the samples edges (the corners of a square specimen in our case). Sample preparation is the following: a thin film of $Ge_2Sb_2Te_5$ was deposited by sputtering onto an inert substrate (SiO_2 on bulk Si); the surface is contacted by four probes by spring-loaded molybdenum contacts. The sample is placed in a vacuum chamber, where pressure has been kept below 0.001 Pa by a turbomolecular pump to prevent oxidation of the sample. The sample holder serves also as a heater stage, to perform in situ measurement of the resistivity as a function of temperature. The temperature profile is handled by a proportional-integral-derivative (PID) controller, while the electrical measurements are controlled by a LabVIEW-equipped personal computer.

Table 1. Thermal Conductivity and Thermal Interface Resistance for Silicon Dioxide, Silicon Nitride, and $Ge_2Sb_2Te_5$ Chalcogenide in the Amorphous, *fcc* and, *hcp* Phases

	thermal conductivity	thermal interface resistance
	$[W \cdot mK^{-1}]$	$[m^2K \cdot W^{-1}]$
SiO_2	1.46	$20 \cdot 10^{-9}$
Si_3N_4	1.45 ± 0.03	$(40 \pm 2) \cdot 10^{-9}$
amorphous GST	0.21 ± 0.02	$(94 \pm 37) \cdot 10^{-9}$
fcc GST	0.55 ± 0.03	$(72 \pm 20) \cdot 10^{-9}$
hcp GST	1.13 ± 0.11	$(159 \pm 11) \cdot 10^{-9}$

Results and Discussion

The thermal characterization was performed on the following materials: SiO_2, Si_3N_4, amorphous GST, face-centered cubic (*fcc*) GST, and hexagonal close packed (*hcp*) GST. The first samples to be examined were the silicon dioxide and silicon nitride thin films. SiO_2 was measured both to validate the experimental setup and because the measured thermal conductivity value of SiO_2 was needed for the calculation of GST conductivity, as discussed in the previous section. The thickness of the samples ranged from (80 to 400) nm for SiO_2 and from (60 to 200) nm for Si_3N_4. The measured values for the two insulators are shown in Table 1.

The obtained values for silicon dioxide are very close to the bulk value[8] 1.37 $W \cdot mK^{-1}$ and to other measurements performed on thin films with different techniques: 1.4 $W \cdot mK^{-1}$ by Lee et al.[9] and (1.35 to 1.55) $W \cdot mK^{-1}$ by Okuda et al.[10] Silicon nitride thermal conductivity is more dependent on the deposition method, the reported values ranging from 1.5 $W \cdot mK^{-1}$ [Lee et al.[11]] to 4.5 $W \cdot mK^{-1}$ [Eriksson et al.[12]]. The measurement also reveals information on the effect of interfaces between the layers on the heat transport. Interface thermal resistance is lowest for the SiO_2 sample, as expected, since the SiO_2/Si interface is known to contain a very low amount of interfacial defects. In the same work by Lee et al.,[11] similar values are reported for thermal boundary resistance between the dielectric (SiO_2 or Si_3N_4) layer and the Si substrate ($R_i \approx 20 \cdot 10^{-9}$ $m^2K \cdot W^{-1}$). In conclusion, it can be stated that the value $R_i = 20 \cdot 10^{-9}$ $m^2K \cdot W^{-1}$ found for the SiO_2 sample represents the contribution of the thermal resistance of the interfaces between both the metal strip and the SiO_2 layer and between the SiO_2 film and the Si substrate. It is expected that the value of the interfacial resistance will never be lower than that for a more complex stack of thin films.

The thermal conductivity of GST (in its three phases) has been measured. Sample thicknesses ranged from (40 to 400) nm. The thermal resistance as a function of thickness for the three sets of samples is shown in Figure 3. Experimental results are shown in Table 1.

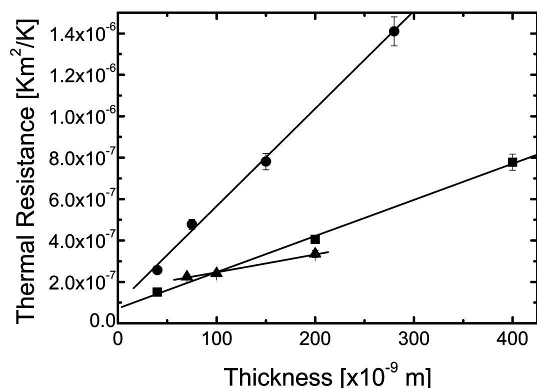

Figure 3. Thermal resistance of ●, amorphous; ■, *fcc*; ▲, and *hcp* $Ge_2Sb_2Te_5$ thin films, as a function of the layer thickness. The intercept to the *y*-axis of the linear fit to the data represents the thermal interfacial resistance.

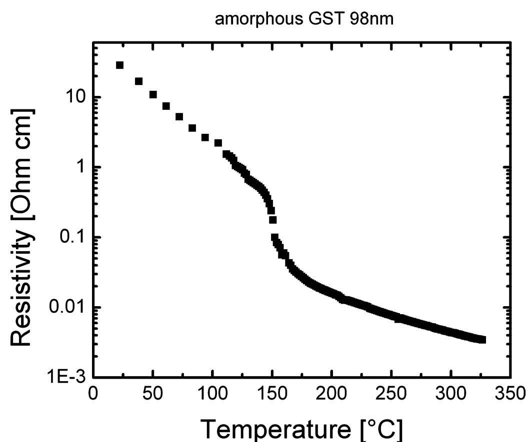

Figure 4. GST electrical resistivity during heating at a constant heating rate of 10 °C·min^{-1} of amorphous as-deposited sample.

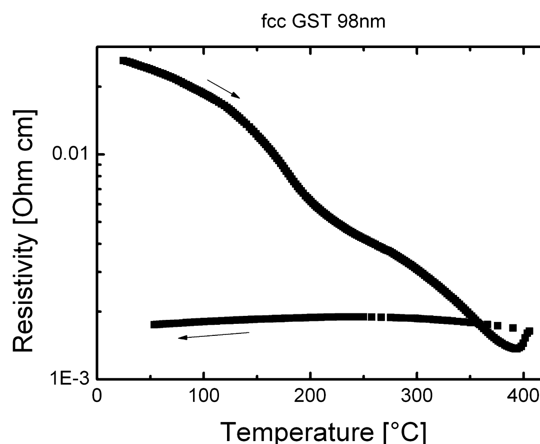

Figure 5. GST electrical resistivity during heating at a constant heating rate of 10 °C·min^{-1} of *fcc* as-deposited sample.

Thermal transport improves from the amorphous to the cubic phase and reaches a maximum for the hexagonal phase, consistent with the increasing effect of electronic heat transport.

The interface thermal resistance of amorphous and *fcc* GST are the same within the experimental error. In contrast, the set of hexagonal-phase GST samples was achieved by thermal annealing in a vacuum, at 350 °C for 30 min, of *fcc* as deposited samples. The process resulted in a worsening of the layer roughness, revealed by a worse adhesion of the evaporated metallization. Actually, the reduction of the layer thickness from the *fcc* to the *hcp* phase due to a denser arrangement of the layer (investigated by Njoroge et al.[13]) causes an increase in the roughness and contributes to the higher value of the measured thermal interface resistance.

Lyeo et al.[14] report values similar to ours for GST thermal conductivity: 0.19 W·mK^{-1} for the amorphous phase, 0.57 W·mK^{-1} for the cubic phase, and 1.58 W·mK^{-1} for the hexagonal phase (measurement obtained by time-domain thermoreflectance). Reifenberg et al.[15] for a 350 nm thick sample specify a thermal conductivity of (0.29, 0.42, and 1.76) W·mK^{-1} for the amorphous, *fcc*, and *hcp* phases, respectively; these values were obtained by laser reflectance thermometry. In another work by Kuwahara et al.,[16] the calculated thermal conductivity of a 300 nm thick RF-sputtered $Ge_2Sb_2Te_5$ film, after 1 h annealing at 350 °C, is reported to be in the (1.15 to 1.3) W·mK^{-1} range (before and after a subsequent measurement at 400 °C).

Electrical resistivity has been evaluated, as a function of temperature, for the phase change material GST. The objective of the experiment was to determine the initial resistivity of the amorphous phase and track its evolution by heating, up to phase transitions and beyond. Since the material presents two-phase transitions, we performed two measurements.

The first measurement has been done on an amorphous as-deposited GST sample, of thickness 98 nm, while heating at constant rate of 10 °C·min^{-1} to observe the transition toward the cubic phase. The resulting plot is shown in Figure 4. Initial resistivity at room temperature was high, as expected for the amorphous state ($\rho = 70$ Ω·cm). It slowly starts to decrease during heating, up to 150 °C, when a sharp drop can be noticed; this is the characteristic temperature of the phase transition. Cooling of the sample started at 325 °C. After the experiment, the cubic phase of the layer was examined and confirmed by structural analysis (performed by X-ray diffraction, not shown here); the final resistivity was $\rho = 0.000\ 4$ Ω·cm.

The second measurement was performed on an *fcc* as-deposited GST sample, of thickness 70 nm, under a constant heating rate of 10 °C·min^{-1}. The resulting plot is shown in Figure 5. As temperature increases, a drop in resistivity can be noticed, from $\rho = 0.03$ Ω·cm to $\rho = 0.001\ 8$ Ω·cm, corresponding to the phase transition to *hcp* (confirmed by XRD). For temperatures higher than 390 °C, the resistivity increases too, owing to the onset of the evaporation of the GST layer. During cooling, the trend is metallic-like (resistivity decreases for decreasing temperature) as expected for the hexagonal phase.

Njoroge et al.[13] and Friedrich et al.[17] performed similar measurements on GST electrical resistivity as a function of temperature. Measured values are consistent with the one presented in this work: some tens of Ω·cm for the amorphous phase, (0.01 to 0.03) Ω·cm for the cubic phase, and 0.000 1 Ω·cm for the hexagonal phase. Characteristic temperatures range from (150 to 160) °C and from (340 to 370) °C for transition toward the *fcc* and *hcp* phases, respectively.

The uncertainty associated with the measurement values reported throughout this work has been estimated by statistical methods (type A of the ISO guide): for each measurement it was assumed that the measured values were approximately normally distributed. The numbers following the symbol ± represent expanded uncertainties with a confidence level of 99 % (coverage factor $k = 2.576$).

Conclusions

Thermal conductivity measurements by the 3ω method performed on thin films of various materials have provided

quantitative information on their conductivity as well as on the interfacial resistance between multilayered structures. The latter, in particular, has been found to vary from a minimum value for the SiO_2/Si interface to higher values for the Si_3N_4/Si layer and highest for the GST/SiO_2/Si interfaces whose dependence on the phase of the chalcogenide has been investigated. The electrical resistivity measurement implemented by the four-point van der Pauw geometry confirmed the trend of GST thin film electrical resistivity as a function of the temperature and its transition temperatures at (150 and 340) °C.

Acknowledgment

The authors would like to acknowledge Maurizio Henin (STMicroelectronics M6[#]) for sample preparation.

Supporting Information Available:

XRD data for the *fcc* to *hcp* transition. This material is available free of charge via the Internet at http://pubs.acs.org.

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Received for review October 17, 2008. Accepted March 7, 2009. This work has been partially supported by the EU Project CHEMAPH (IST-027561) within the sixth Framework Programme and by the national FIRB project.

JE800770S